primary chip body while contacting the wire connecting portion and the electrical contact projection in a surrounding manner such that a segment of the wire connecting portion and a segment of the electrical contact projection project from the surface protective film, wherein

the electrical contact projection is in a form of a bump and the wire connecting portion substantially has a shape of the bump.

Please add new claims 13 and 14 as follows:

-- 13. (NEW) The semiconductor chip according to claim 11, wherein the wire connection portion and the electrical contact projection are made of the same material and have simultaneously been formed.

14. (NEW) The semiconductor chip according to claim 12, wherein the wire connection portion and the electrical contact projection are made of the same material and have simultaneously been formed. --

REMARKS

Reexamination and reconsideration in light of the above amendments and the following remarks are courteously requested.

Claims 2-5, 7 and 10-14 are pending in the application. By this Amendment, claims 11 and 12 are amended and claims 13 and 14 are added.

Claim 11 is rejected under 35 U.S.C. 103(a) as unpatentable over Idaka et al. (U.S. Patent No. 5,587,337) in view of Eldridge et al. (U.S. Patent No. 6,032,356). The rejection is respectfully traversed.

Claim 11 is directed to a semiconductor chip adapted for electrical connection to an external terminal and includes a semiconductor chip body, a wire connecting portion, an electrical contact projection, a surface protective film and a wire. Claim 11 recites that the semiconductor chip body has a surface with internal wiring disposed thereon, at

least one surface area of the internal wiring defining an external connection pad and at least one other surface area different from the at least one surface area of the internal wiring defining an internal connection pad with both the external connection pad and the internal connection pad facing in a same direction as the surface of the semiconductor chip body. Claim 11 is also recites that the wire connecting portion is fabricated from a metal material having oxidation resistance and is electrically connected to the external connection pad. Claim 11 recites that the electrical contact projection is fabricated from a metal material having oxidation resistance and electrically connected to the internal connection pad. Furthermore, claim 11 recites that the surface protective film covers the internal wiring and the surface of the semiconductor chip body while contacting the wire connecting portion and the electrical contact projection in a surrounding manner such that a segment of the wire connecting portion and a segment of the electrical contact projection project from the surface protective film. Additionally, claim 11 recites that the wire is electrically connected to the segment of the wire connecting portion for connecting the semiconductor chip to the external terminal. Further, claim 11 recites that the electrical contact projection is in a form of a bump and the wire connecting portion substantially has a shape of the bump.

Idaka discloses a semiconductor device for use in a TAB mounting technique. In this device, a LSI chip 1 is covered with a passivation film 13 which has an opening 13a where a pad 12 of aluminum is exposed. A bump electrode 3 made of gold, for example, is provided so as to cover the opening 13a. It is also disclosed that the bump electrode 3 may be formed by way of gold plating.

Eldridge discloses a wire 320 connected to a portion 315 of a metal blanket layer 310. However, Eldridge fails to disclose an electrical contact projection which is connected to an internal connection pad, in addition to the portion 315. Moreover, Eldridge fails to disclose a wire connecting portion that substantially has a shape of a bump.

It is respectfully submitted that none of the applied art, alone or in combination, teaches or suggests the features of claim 11 as mentioned above. Thus, it is respectfully submitted that one of ordinary skill in the art would not be motivated to

combine the features of the applied art because such combination would not result in the claimed invention. As a result, it is respectfully submitted that claim 11 is allowable over the applied art.

Withdrawal of the rejection is respectfully requested.

Claims 2, 3 and 4 are rejected under 35 U.S.C. 103(a) as unpatentable over Idaka in view of Eldridge as applied to claim 11 and further in view of Kawakita (U.S. Patent No. 5,734,199). The rejection is respectfully traversed.

Kawakita discloses a semiconductor chip 120 which has bumps 123 for connection with another semiconductor chip 110 as well as bumps 124 which are not used for connection with the semiconductor chip 110. However, Kawakita never suggests a wire bonded to the bumps 124.

As discussed above, claim 11 is allowable over Idaka and Eldridge. Kawakita fails to cure the deficiencies of Idaka and Eldridge. Thus, claim 11 is allowable over the combination of these references.

Claims 2, 3 and 4 depend from claim 11 and include all of the features of claim 11. Thus, it is respectfully submitted that the dependent claims are allowable at least for the reason claim 11 is allowable as well as for the features they recite.

Withdrawal of the rejection is respectfully requested.

Claim 5 is rejected under 35 U.S.C. 103(a) as unpatentable over Idaka and Eldridge as applied to claim 11 and further in view of Hayashida et al. (U.S. Patent No. 6,060,768). The rejection is respectfully traversed.

Hayashida teaches a semiconductor device with wire connection portions.

As discussed above, claim 11 is allowable over Idaka and Eldridge. Hayashida fails to cure the deficiencies of Idaka and Eldridge. Thus, claim 11 is allowable over the combination of these references.

Claims 5 depends from claim 11 and include all of the features of claim 11. Thus, it is respectfully submitted that the dependent claim is allowable at least for the reason claim 11 is allowable as well as for the features they recite.

Withdrawal of the rejection is respectfully requested.

Claims 7, 10 and 12 are rejected under 35 U.S.C. 102(b) as anticipated by

Japan Patent Abstract Publication 2000-234904. The rejection is respectfully traversed.

Japan 904 teaches a semiconductor device having a chip-on-chip structure.

Claim 12 is directed to a semiconductor device having a chip-on-chip structure in which a secondary chip is overlapped with and joined to a primary chip. Claim 12 recites that the primary chip comprises a primary chip body, a wire connecting portion, an electrical contact projection and a surface protective film. Claim 12 recites that the primary chip body has a surface with internal wiring disposed thereon, at least one surface area of the internal wiring defining an external connection pad and at least one other surface area different from the at least one surface area of the internal wiring defining an internal connection pad with both the external connection pad and the internal connection pad facing in a same direction as the surface of the primary chip body. Claim 12 recites that the wire connecting portion is fabricated from a metal material having oxidation resistance and is electrically connected to the external connection pad. Claim 12 also recites that the electrical contact projection is fabricated from a metal material having oxidation resistance and is electrically connected to the internal connection pad with the electrical contact projection operative to electrically connect the primary and secondary chips together. Further, claim 12 recites that the surface protective film covers the internal wiring and the surface of the primary chip body while contacting the wire connecting portion and the electrical contact projection in a surrounding manner such that a segment of the wire connecting portion and a segment of the electrical contact projection project from the surface protective film. Additionally, claim 12 recites that the electrical contact projection is in a form of a bump and the wire connecting portion substantially has a shape of the bump.

It is respectfully submitted that none of the applied art, alone or in combination, teaches or suggests the features of claim 12. Specifically, none of the applied art, alone or in combination, teaches or suggests an electrical contact projection is in a form of a bump and a wire connecting portion substantially has a shape of the bump.. Thus, it is respectfully submitted that one of ordinary skill in the art would not be motivated to combine the features of the applied art because such combination would not result in

the claimed invention. As a result, it is respectfully submitted that claim 12 is allowable over the applied art.

Claims 7 and 10 depend from claim 12 and include all of the features of claim 12. Thus, it is respectfully submitted that the dependent claims are allowable at least for the reason claim 12 is allowable as well as for the features they recite.

Withdrawal of the rejection is respectfully requested.

Newly-added claims 13 and 14 also include features not shown in the applied art.

In view of the foregoing, reconsideration of the application and allowance of the pending claims are respectfully requested. Should the Examiner believe anything further is desirable in order to place the application in even better condition for allowance, the Examiner is invited to contact Applicant's representative at the telephone number listed below.

Should additional fees be necessary in connection with the filing of this paper or if a Petition for Extension of Time is required for timely acceptance of the same, the Commissioner is hereby authorized to charge Deposit Account No. 18-0013 for any such fees and Applicant(s) hereby petition for such extension of time.

Respectfully submitted,

Date: May 15, 2003

By: _____
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Enclosure(s): Appendix I (Marked-Up Version of Amended Claims)
Petition for Extension of Time (three months)

DC121062

APPENDIX I

(MARKED-UP VERSION OF AMENDED CLAIMS)

11. (Amended) A semiconductor chip adapted for electrical connection to an external terminal, comprising:

a semiconductor chip body having a surface with internal wiring disposed thereon, at least one surface area of the internal wiring defining an external connection pad and at least one other surface area different from the at least one surface area of the internal wiring defining an internal connection pad, both the external connection pad and the internal connection pad facing in a same direction as the surface of the semiconductor chip body;

a wire connecting portion fabricated from a metal material having oxidation resistance and electrically connected to the external connection pad;

an electrical contact projection fabricated from a metal material having oxidation resistance and electrically connected to the internal connection pad;

a surface protective film covering the internal wiring and the surface of the semiconductor chip body while contacting the wire connecting portion and the electrical contact projection in a surrounding manner such that a segment of the wire connecting portion ~~projects~~ and a segment of the electrical contact projection project from the surface protective film; and

a wire electrically connected to the segment of the wire connecting portion for connecting the semiconductor chip to the external terminal, wherein

the electrical contact projection is in a form of a bump and the wire connecting portion substantially has a shape of the bump.

12. (Amended) A semiconductor device having a chip-on-chip structure in which a secondary chip is overlapped with and joined to a primary chip, wherein

said primary chip comprises

a primary chip body having a surface with internal wiring disposed thereon, at least one surface area of the internal wiring defining an external connection

pad and at least one other surface area different from the at least one surface area of the internal wiring defining an internal connection pad, both the external connection pad and the internal connection pad facing in a same direction as the surface of the primary chip body;

a wire connecting portion fabricated from a metal material having oxidation resistance and electrically connected to the external connection pad;

an electrical contact projection fabricated from a metal material having oxidation resistance and electrically connected to the internal connection pad, the electrical contact projection operative to electrically connect the primary and secondary chips together; and

a surface protective film covering the internal wiring and the surface of the primary chip body while contacting the wire connecting portion and the electrical contact projection in a surrounding manner such that a segment of the wire connecting portion and a segment of the electrical contact projection project from the surface protective film, wherein

the electrical contact projection is in a form of a bump and the wire connecting portion substantially has a shape of the bump.